[Document Name] Specification

[Title of the Invention] OVERLAY MARK, METHOD OF MEASURING OVERLAY ACCURACY, METHOD OF MAKING ALIGNMENT AND SEMICONDUCTOR DEVICE THEREWITH

[Claims]

[Claim 1] An overlay mark having a mark pattern formed by engraving a groove or an indent in a prescribed position on a layer where a circuit pattern is formed, and a grooved pattern that surrounds said mark pattern so as to protect said mark pattern from being deformed by thermal expansion or contraction of said layer.

[Claim 2] An overlay mark used for measuring the overlay accuracy in forming a second circuit pattern over a first circuit pattern; which has:

a first lower-layer pattern formed by engraving a groove or an indent in a prescribed position on a first layer where the first circuit pattern is formed, and an upper-layer pattern formed in a prescribed position on a second layer where the second circuit pattern is to be formed; and, in addition,

a second lower-layer pattern that is formed by engraving, on the first layer, a frame-shaped groove to surround the first lower-layer pattern, and is not used for measuring the overlay accuracy.

[Claim 3] The overlay mark according to Claim 2, wherein the first lower-layer pattern is utilized as an alignment mark at the time of alignment to superimpose a mask onto

a wafer in the step of exposure.

[Claim 4] The overlay mark according to Claim 2 or 3; wherein:

the first lower-layer pattern is either a grooved pattern in the shape of a polygonal frame viewed from the top or a polygonal depressed pattern; and

the second lower-layer pattern is a grooved pattern in the shape of a polygonal frame viewed from the top, being formed to surround the first lower-layer pattern at a substantially equal interval.

[Claim 5] The overlay mark according to Claim 2 or 3; wherein:

the first lower-layer pattern is a grooved pattern in which, viewed from the top, a pair of bar-shaped patterns are arranged parallel, facing each other with the upper-layer pattern between; and

the second lower-layer pattern is a grooved pattern in the shape of a quadrangular frame viewed from the top, and is formed to surround the whole of the first lower-layer pattern, wherein sides of said frame-shaped grooved pattern running parallel to respective bar-shaped patterns in the first lower-layer pattern are disposed at an equal interval to the corresponding opposite bar-shaped pattern.

[Claim 6] The overlay mark according to Claim 2 or 3; wherein:

the first lower-layer pattern is a grooved

pattern in which, viewed from the top, a pair of bar-shaped patterns are arranged parallel, facing each other with the upper-layer pattern between; and

the second lower-layer pattern is a grooved pattern comprising patterns, each in the shape of a quadrangular frame viewed from the top and formed to surround respective bar-shaped patterns of the first lower-layer pattern, wherein sides of said frame-shaped grooved pattern running parallel to respective bar-shaped patterns in the first lower-layer pattern are disposed at an equal interval to the corresponding opposite bar-shaped pattern.

[Claim 7] The overlay mark according to Claim 5; which has a third lower-layer pattern, in a region surrounded by the second lower-layer pattern on the first layer, formed by engraving grooves to surround every bar-shaped pattern of the first lower-layer pattern separately, each in the shape of a frame; wherein:

sides of third lower-layer pattern running parallel to respective bar-shaped patterns in the first lower-layer pattern are disposed at an equal interval to the corresponding opposite bar-shaped pattern; while

the third lower-layer pattern is not used for measuring the overlay accuracy.

[Claim 8] The overlay mark according to any of Claims 1-7, wherein said upper-layer pattern is formed from a resist layer laid over the second layer and comprises a

pattern in the shape of a polygon, a frame or a bar viewed from the top.

[Claim 9] An overlay mark used for making alignment to detect and decide an aligning position of a wafer and a mask, in the step of exposure during photolithography to form a second circuit pattern over a first circuit pattern; which has:

a first pattern formed by engraving a groove or an indent in a prescribed position on a layer where the first circuit pattern is formed; and

a second pattern that is formed by engraving a frame-shaped groove to surround the first pattern, and is not used for making alignment.

[Claim 10] The overlay mark according to Claim 9; wherein:

the first pattern is a grooved pattern in the shape of a polygonal frame viewed from the top; and

the second pattern is a grooved pattern in the shape of a polygonal frame viewed from the top, being formed to surround the first pattern at a substantially equal interval.

[Claim 11] The overlay mark according to Claim 9; wherein:

the first pattern is a grooved pattern in which, viewed from the top, bar-shaped patterns are arranged parallel; and

the second pattern is a grooved pattern in the

shape of a quadrangular frame viewed from the top, and is formed to surround the whole of the first pattern, wherein sides of said frame-shaped grooved pattern running parallel to respective bar-shaped patterns in the first pattern are disposed at an equal interval to the corresponding opposite bar-shaped pattern.

[Claim 12] The overlay mark according to Claim 9; wherein:

the first pattern is a grooved pattern in which, viewed from the top, bar-shaped patterns are arranged parallel; and

the second pattern is a grooved pattern comprising patterns, each in the shape of a quadrangular frame viewed from the top and formed to surround respective bar-shaped patterns of the first pattern, wherein sides of said frame-shaped grooved pattern running parallel to respective bar-shaped patterns in the first pattern are disposed at an equal interval to the corresponding opposite bar-shaped pattern.

[Claim 13]The overlay mark according to Claim 11; which has a third pattern, in a region surrounded by the second pattern on the layer where the first circuit pattern is formed, formed by engraving grooves to surround every bar-shaped pattern of the first pattern separately, each in the shape of a frame; wherein:

sides of third pattern running parallel to respective bar-shaped patterns in the first pattern are

disposed at an equal interval to the corresponding opposite bar-shaped pattern; while

the third pattern is not used for making alignment.

[Claim 14] The overlay mark according to Claim 11, 12 or 13, wherein, in place of said bar-shaped pattern, a pattern in which quadrangular indents are arranged in a line is formed.

[Claim 15] A semiconductor device having a substrate on which the overlay mark according to any of Claims 1 - 14 is formed.

[Claim 16] A method of measuring the overlay accuracy in forming a second circuit pattern over a first circuit pattern, wherein the overlay mark according to any of Claims 2 - 8 is used but, at least, the outermost lower-layer pattern is not utilized to detect an overlay position.

[Claim 17] A method of making alignment to detect and decide an aligning position of a wafer and a mask, in the step of exposure during photolithography to form a second circuit pattern over a first circuit pattern, wherein the overlay mark according to any of Claims 9 - 14 is used but, at least, the outermost pattern is not utilized to detect an aligning position.

[Detailed Description of the Invention]

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[Field of the Invention]